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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,755	09/11/2006	Bartlomiej Jan Pawlak	NL040276	9871

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EXAMINER	
HUNG, MING HUNG	

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/598,755	PAWLAK, BARTLOMIEJ JAN	
	Examiner	Art Unit	
	MING HUNG HUNG	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Preliminary amendment received on 09/11/06 has been entered into record.

2. Claims 1-11 are pending.

Priority

3. Examiner acknowledged that this application 10/598,755 filed on 09/11/06 claims the benefit of the foreign application EPO 04101071.1 filed on 03/16/04. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. Page 4, line 11, “en” should read “and”. Appropriate action is required.

Claim Objections

6. Claim 7 is objected to because line 4 “en” should read “and”. Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-7, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over An et al. (US Patent No. 6,245,618 B1, Applicant's admitted prior art, and An hereinafter) in view of Wu (US Patent No. 5,773,348).

9. As to claims 1 and 7, An discloses:

a method of manufacturing a semiconductor device (10) comprising a field effect transistor (col. 1, lines 6-11)**, in which method a semiconductor body (1) of silicon** (semiconductor substrate 50, Figs. 5-17; it is well known that silicon is commonly used as the substrate) **is provided at a surface thereof with a source region (2) and a drain region (3) of a first conductivity type** (n-type source/drain regions 80, Figs. 8-17; col. 3, lines 28-29)**, which regions are both provided with extensions (2A,3A)** (source/drain extensions 60, Figs. 6-17; col. 3, lines 22-24)**, and with a channel region (4) of a second conductivity type, opposite to the first conductivity type, between the source region (2) and the drain region (3)** (the space between source/drain extensions 60 as shown in Figs. 12-17, which is a p-type semiconductor substrate 50; col. 3, lines 20-22)**, and with a gate region (5)** (gate electrode 170, Fig. 17) **separated from the surface of the semiconductor body (1) by a gate dielectric (6)** (gate dielectric layer 150, Fig. 17) **and situated above the channel region (4)** (Fig. 17)**, and where a pn-junction between the extensions**

(2A,3A) (there is a pn junction between the source/drain extensions 60 since the source/drain extensions 60 are n-type and the semiconductor substrate 50 is p-type) **and a neighboring part (4A)** (retrograde impurity region 130, Figs. 13-17) **of the channel region (4)** (retrograde impurity region 130, Figs. 13-17) **is formed by two implantations (I_1, I_2)** (Figs. 6 and 8 together formed the first implantation in the source/drain extensions 60 and regions 80 and Figs. 12 and 13 together formed the second implantation under the gate region, and the retrograde impurity region 130 is formed in Fig. 13, which is part of the second implantation that is part of the two implantations) **of dopants of opposite conductivity type** (the retrograde impurity region 130 in the second implantation has p-type conductivity opposite to the n-type source/drain extensions 60 and regions 80 in the first implantation; col. 3, lines 22-24, 28-29, 60-61)**, and characterized in that the amorphizing implantation (I_0) and the two implantations (I_1, I_2) of dopants of opposite conductivity type are performed before the gate region (5) is formed** (everything is formed before the gate electrode 170 is formed in Fig. 17) **and at an angle with the surface of the semiconductor body (1) which is substantially equal to 90 degrees** (all the implantations are 90 degrees as shown in Figs. 6, 8, 12 and 13) **[claim 1]**.

However, An fails to disclose:

where before both of the two implantations (I_1, I_2) of dopants of opposite conductivity type are performed an amorphizing implantation (I_0) is performed where the pn-junction is to be formed [claim 1];

characterized in that the first and second implantations (I_1, I_2) are annealed at a temperature between 500 en 700 degrees [claim 7].

Nonetheless, these features are well known in the art and would have been an obvious modification of the method disclosed by An, as evidenced by Wu.

Wu discloses:

where before both of said two implantations (I_1, I_2) of dopants of opposite conductivity type are performed an amorphizing implantation (I_0) is performed where the pn-junction is to be formed (doped region 28 in Fig. 4 is performed before the lightly-doped areas 36 and the heavily-doped areas 42 in Figs. 9 and 11) **[claim 1]** to prevent punch through effect**;**

characterized in that the first and second implantations (I_1, I_2) are annealed at a temperature between 500 en 700 degrees (col. 6, lines 3-4; Fig. 11) **[claim 7]** to form short channel**.**

Given the teaching of Wu, a person having ordinary skills in the art at the time of invention would have readily recognized the desirability and advantages of modifying An by employing the well known and conventional feature of having the amorphizing implantation performed before the two implantations and annealing at a temperature between 500 and 700 degrees, such as disclosed by Wu, in order to provide a fabricating method which can extend the limit of the current lithographic process and prevent the substrate from being damage by some etching process.

10. As to claims 2-4, 9-11, An also discloses:

characterized in that a first implantation (I_1) (Fig. 6 and 8 together formed the first implantation in the source/drain extensions 60 and regions 80) **of the two opposite conductivity type implantations (I_1,I_2)** (the retrograde impurity region 130 formed in the second implantation has p-type conductivity opposite to the n-type source/drain extensions 60 and regions 80 formed in the first implantation; col. 3, lines 28-29, 60-61) **is carried out using a first mask (M_1)** (temporary gate electrode 54, Figs. 6 and 8) **covering a first region of the semiconductor body (1)** (covers the region below the temporary gate electrode 54 as shown in Figs. 6 and 8**) and the second implantation (I_2) is carried out after removal of the first mask (M_1)** (Figs. 12 and 13 are performed after the temporary gate electrode 54 is removed in Fig. 11)**, using a second mask (M_2)** (dielectric layer 90, Fig. 9) **of which the edge coincides with the edge of the first mask (M_1)** (the temporary gate electrode 54 and the dielectric layer 90 overlaps as shown in Fig. 9) **[claim 2];**

characterized in that the first mask (M_1) and the second mask (M_2) are formed in a self-aligned manner (Figs. 5 and 10) **[claim 3];**

characterized in that the first mask (M_1) is formed by a dummy gate region (5A) (temporary gate electrode 54 is used and then later removed as shown in Figs. 5-11) **of a first dielectric material** (temporary gate oxide 52, Figs. 10)**, and the first implantation (I_1) is used to form the extensions (2A,3A) of the source and drain regions (2,3)** (Figs. 6 and 8 together formed the first implantation in the source/drain extensions 60 and regions 80) **[claim 4];**

characterized in that for the amorphizing implantation (I_0) ions are chosen from a group comprising Ge, Si, Ar or Xe (col. 3, lines 44-50) **[claim 9];**

characterized in that a part of the function of the amorphizing implantation (I_0) is provided by one of the two opposite conductivity type implantations (I_1,I_2) (buried amorphous region 120 is provided by Fig. 12 of the second implantation) **[claim 10];**

a semiconductor device (10) comprising a field effect transistor obtained with a method as claimed in claim 1 (col. 1, lines 6-11) **[claim 11].**

11. As to claim 5, An discloses substantial features the claim invention (see paragraphs above) and further discloses:

characterized in that after the first implantation (I_1) (Figs. 9-17) **a uniform masking layer (40) of a second dielectric material different from the first dielectric material is deposited on the semiconductor body (1)** (dielectric layer 90, Fig. 9) **and is subsequently removed from the top of the dummy gate region (5A)** (Figs. 9-10; col. 3, lines 35-36) **which is then removed by selective etching** (col. 3, lines 37-38 and col. 4, lines 28-32)**, the remainder of the masking layer (40) forming the second mask (M_2) for the second implantation (I_2)** (dielectric layers 90, Figs. 12-13) **which is used to dope the neighboring part (4A) of the channel region (4)** (retrograde impurity region 130, Fig. 13)**.**

However, An fails to disclose

the subsequent removal of the uniform masking layer (40) from the top of dummy gate region (5A) being chemical mechanical polishing.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by An, based on the information provided by An.

An discloses:

planarizing the surface of a conductive layer using chemical mechanical polishing (col. 4, lines 20-26).

Given the teaching of An, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying the method disclosed by An by employing the well known and conventional feature of chemical mechanical polishing, in order to planarize the dummy gate region using chemical mechanical polishing.

12. As to claim 6, An also discloses:

after the second implantation (I_2), a uniform gate region layer (50) is formed on top of the semiconductor body (I) (conductive layer 160, Fig. 16; Fig 16 is performed after Figs. 12-13) **and is subsequently removed by chemical mechanical polishing from the top of the second mask (M_2) which is then removed by selective etching** (col. 4, lines 20-32)**.**

13. Claim 8 is are rejected under 35 U.S.C. 103(a) as being unpatentable over An in view of Wu as applied to claim 1, and further in view of Lai et al. (US PGPUB 2002/0102801 A1 and Lai hereinafter).

14. As to claim 8, although An discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

characterized in that the source- and drain regions (2,3) are formed before the source- and drain extensions (2A,3A).

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by An in view of Wu, as evidenced by Lai.

Lai discloses:

characterized in that the source- and drain regions (2,3) are formed before the source- and drain extensions (2A,3A) (source/drain regions 108 are formed before the extension 114 is formed as shown in Figs. 1C-1D)**.**

Given the teaching of Lai, a person having ordinary skills in the art a the time of the invention would have readily recognized the desirability and advantages of modifying An in view of Wu by employing the well known or conventional feature of forming the source- and drain regions (2,3) before the source- and drain extensions (2A,3A), such as disclosed by Lai, in order to avoid thermal process.

Contact Information

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ming Hung Hung whose telephone number is (571) 270-3832. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ming Hung Hung/
Examiner, Art Unit 2829
April 11, 2008

/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829